

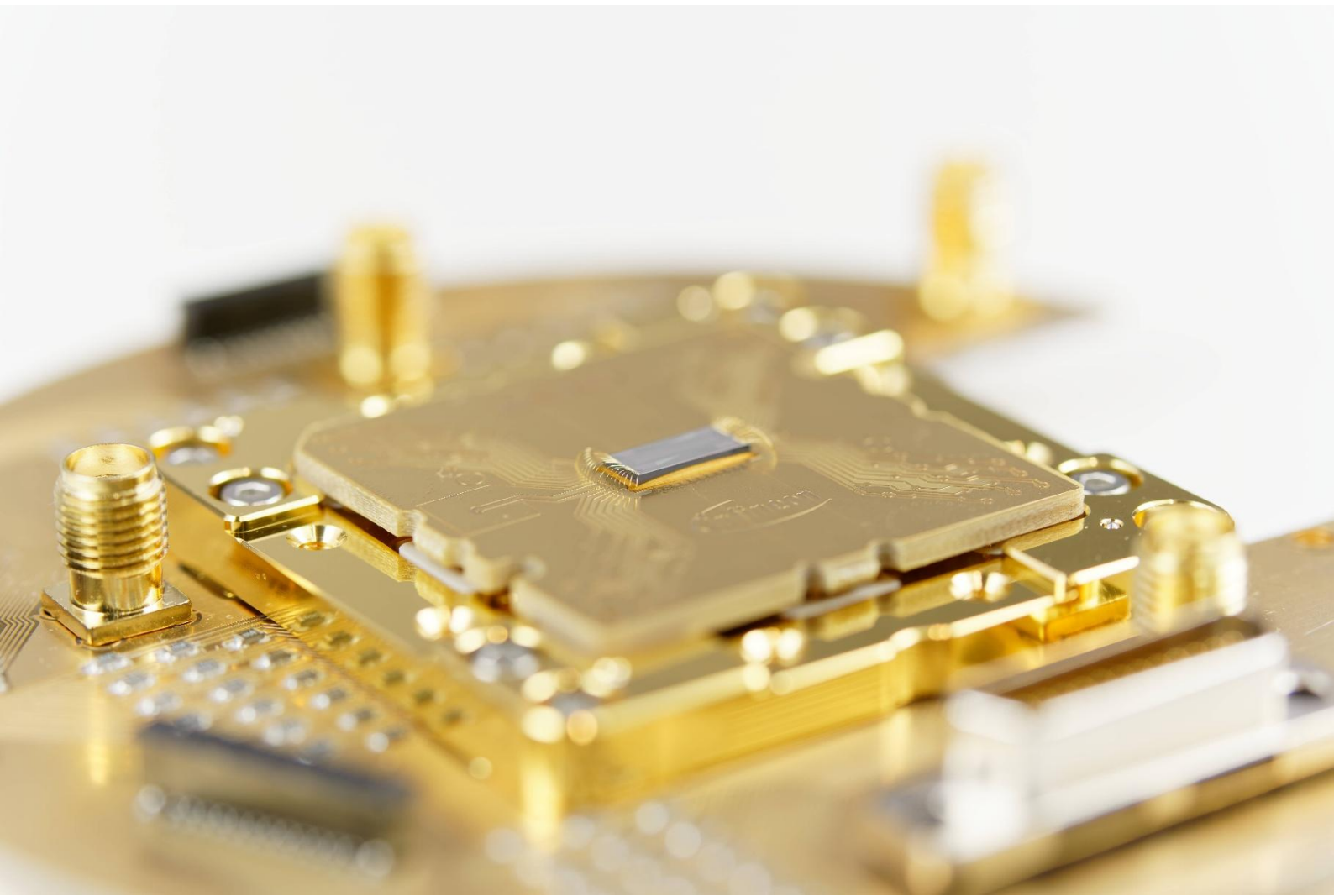
Next generation HPC with quantum bits based on trapped ions

Quantum computing is emerging as an accelerator for problems where classical methods face inherent scaling bottlenecks. The most practical near-term path is hybrid: pair high-performance computing (HPC) with a quantum processing unit (QPU) to execute the specific quantum subroutines while classical nodes handle data-heavy numerics, orchestration, and post-processing. Among the candidate quantum platforms, trapped ions stand out for long coherence times, high-fidelity gates, and flexible connectivity. Europe is investing to integrate quantum capabilities with established HPC infrastructure. Within this landscape, Infineon's Ion Trap Systems (ITS) team focuses on maturing the microfabricated hardware that will translate laboratory breakthroughs into dependable, scalable modules, while programs like ACHIEVE help build the talent pipeline needed to realize this vision.



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A pragmatic path to hybrid HPC–quantum

Hybrid HPC–QPU deployments are already underway in pilot projects and are nearing routine use. This approach makes sense because it matches strengths: HPC excels at large-scale classical compute, data management, and workflow orchestration, while QPUs target subroutines where quantum resources can provide an advantage, from certain sampling tasks to selected optimization or simulation primitives. The result is a division of labor where classical pre/post-processing, calibration, and error mitigation frame relatively short bursts of quantum execution—an operational model compatible with HPC scheduling, observability, and reproducibility practices.

Why quantum computing?

Quantum computing harnesses the fundamental quantum mechanical phenomena of superposition and entanglement to process information in ways fundamentally different from classical computation. Superposition allows quantum bits (qubits) to exist in combinations of 0 and 1 states simultaneously, while entanglement creates correlations between qubits that enable parallel exploration of solution spaces. These quantum states form the foundation for algorithms that can solve certain problems exponentially faster than classical approaches.

Some computational challenges—especially in combinatorial optimization, quantum chemistry for small active spaces, and specific sampling or amplitude-estimation tasks—exhibit scaling behaviors that strain even the largest supercomputers. Quantum algorithms promise asymptotic improvements for well-defined problems. Crucially, quantum advantage is domain-specific and contingent on the interplay of algorithm design, noise characteristics, and system constraints. In practical workflows, classical computation remains substantial, guiding parameter updates, embedding problems into modest-depth circuits, and applying error-mitigation techniques to extract meaningful signals from noisy measurements. These realities underscore why a hybrid path is pragmatic and productive.

Trapped-ion quantum computing: how it works

In trapped ion systems, individual atomic ions are confined above microfabricated chips using electromagnetic fields. Careful chip design and precision voltage waveforms establish stable trapping zones and transport pathways that can be reconfigured on demand.

Qubits are encoded in the ions' internal electronic or hyperfine states. These levels are intrinsically well defined and exhibit long coherence times. Single and two qubit gates are driven by laser beams or microwave fields. Achieving low error rates requires high quality chips as well as precise timing, frequency stabilization, and drift management across lasers, RF sources, and control electronics—a full stack engineering effort spanning microfabrication, optics, electronics, and software.

Connectivity is enabled by shuttling: segmented electrodes move ions between zones to bring desired pairs into interaction range. Because quantum information cannot be copied (the no cloning theorem), architectures rely on moving qubits and swapping operations. The reconfigurable connectivity of trapped ions simplifies compilation compared to strictly nearest neighbor architectures, a practical advantage.

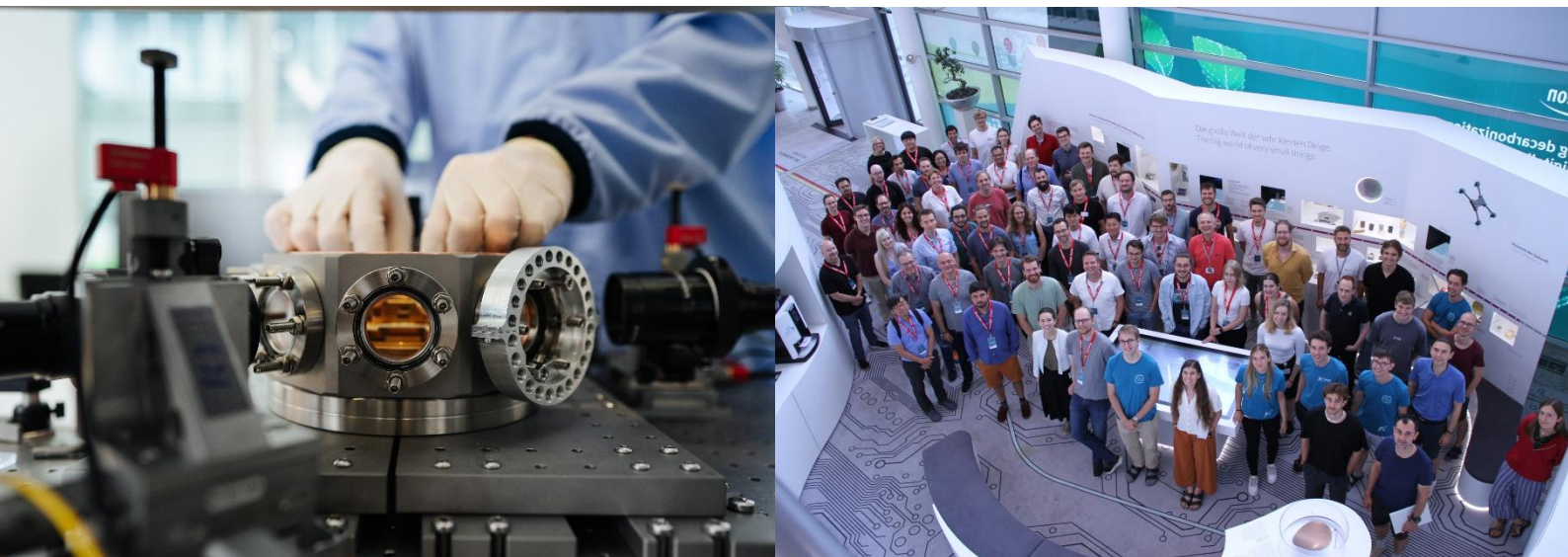


Figure 1: Cryogenic vacuum chamber holding an ion trap in the Quantum Lab of the Ion Trap Systems team (left). Group picture of the Chip trap Workshop 2025 at Infineon in Villach, Austria (right).

Infineon as enabler and European anchor

Infineon's Ion Trap Systems (ITS) team advances microfabricated ion trap chips, integrated photonics, cryogenic control electronics and packaging, working to bridge the gap from academic prototypes to industrial grade modules. The purpose-built quantum lab (Figure 1) allows for quick learning cycles and experimental insights into the design and fabrication of ion traps that would not be feasible in a purely research oriented lab. As part of Europe's semiconductor infrastructure, ITS contributes to regional sovereignty by connecting research labs, startups and industry to enable scalable trapped-ion quantum computers.

A recent example of community engagement is the Chip Trap Workshop 2025, held at the Infineon site in Villach, Austria. Organized by ITS in the context of the ACHIEVE project, the workshop gathered scientists, engineers, and startups in trapped ion quantum computing to foster exchange and collaboration on different topics, especially on ion trap chip design, fabrication, and system integration.

State of the community and the skills required

The field is transitioning from bespoke laboratory devices to systems that begin to show economic value in targeted pilot settings. To broaden impact, the community must scale qubit counts and throughput while retaining high fidelities and reproducibility—an engineering-intensive challenge. Success demands a full-stack approach:

- **Microfabrication and materials:** wafer-level consistency, surface quality, and integration of active elements, transistors and photonic modulators, near the trap.
- **Control electronics:** cryogenic DACs, multiplexers, and RF circuits.
- **Photonics and lasers:** stabilized light sources, integrated optics, and robust packaging.
- **Software stack:** compilers & frameworks compatible with HPC practices.
- **Systems and facilities:** vacuum & cryogenics, vibration isolation, and thermal management.

This convergence mirrors the multidisciplinary nature of modern HPC centers, where chip manufacturing and design, electrical engineering, systems engineering (including compilers and low-level firmware), and mechanical engineering all intersect. Quantum computing adds device physics and precision controls to that mix, creating a rich environment for cross-disciplinary training and collaboration. Europe's momentum in hybrid HPC-quantum integration depends on cultivating talent that understands both physics and engineering.

Programs such as ACHIEVE provide hands-on exposure through internships and thesis projects. In parallel, Infineon's ITS team is building a European anchor for trapped-ion technology and welcomes interest from students and researchers across multiple disciplines. Opportunities include internships, master's theses, summer schools, PhD projects, and staff roles in all areas mentioned above.

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